ABSTRACT

According to one exemplary embodiment, a floating gate memory cell comprises a stacked gate structure situated on a substrate and situated over a channel region in the substrate. The floating gate memory cell further comprises a recess formed in the substrate adjacent to the stacked gate structure, where the recess has a sidewall, a bottom, and a depth. According to this exemplary embodiment, the floating gate memory cell further comprises a source situated adjacent to the sidewall of the recess and under the stacked gate structure. The floating gate memory cell further comprises a Vss connection region situated under the bottom of the recess and under the source, where the Vss connection region is connected to the source. The Vss connection region being situated under the bottom of the recess causes the source to have a reduced lateral diffusion in the channel region.

Figure 2C should accompany the Abstract.